Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WEI-MUN CHU, SUDHAKAR R. GOURAVARAM
and SON NGUYEN

Appeal No. 2002-0286
Application No. 09/113,995

ON BRIEF

Before KRASS, BARRETT and SAADAT, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-30, all of the pending claims.

The invention is directed to integrated circuit design. In particular, in a technique for the placement and routing of circuits during an integrated circuit design, a single cell includes both a signal processing circuit and a buffer circuit for buffering a signal external to the integrated circuit in which the cell is included. This is said to result in a

simplified layout and routing with respect to certain signal processing circuits.

Representative independent claim 19 is reproduced as follows:

19. A cell library for use in designing integrated circuits, comprising:

a cell which includes (1) a signal processing circuit; (2) a buffer circuit for buffering a signal external to an integrated circuit in which said cell is to be included; and (3) layout information for specifying a layout of an interconnecting trace between said signal processing circuit and said buffer circuit.

The examiner relies on the following references:

Smith et al. (Smith)	5,247,668	Sep. 21, 1993
Tanaka et al. (Tanaka)	5,737,237	Apr. 07, 1998
Kawakami	5,774,371	Jun. 30, 1998
Varadarajan et al. (Varadarajan)	5,838,583	Nov. 17, 1998 (filed Apr. 12, 1996)
Luk et al. (Luk)	5,883,814	Mar. 16, 1999 (filed Mar. 13, 1997)

Claims 1-30 stand rejected under 35 U.S.C. §102(e) as anticipated by any one of Luk or Varadarajan or Tanaka or Kawakami.

Claims 1-30 stand further rejected under 35 U.S.C. §102(b) as anticipated by Smith.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed sub nom., Hazeltine Corp. v. RCA Corp., 468 U.S. 1228 (1984); W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

Each of the instant claims on appeal requires, in one form or another, that a single cell includes a signal processing circuit, a buffer circuit for buffering a signal external to the integrated circuit in which the cell is included, and layout information.

The examiner points to a total of five different references and alleges that any one of these references anticipates the instant claimed invention. However, while the examiner ostensibly lists how each reference has elements therein which correspond to the instant claimed elements (see pages 5-6 of the answer), this list, along with the examiner's explanations, is

nothing more than a reference to various parts of the references, with no explanation whatsoever as to how each and every claim limitation is alleged to be met.

For example, at page 5 of the answer, with reference to Luk, the examiner points to the abstract, Figures 2, 4A-4D and 6-14, the summary of the invention, column 5, lines 29 et seq. and column 7, lines 1-3, of Luk, offering portions relating to synthesizing buffers, drivers and latches in accordance with input requirements for the function of a chip, DSP, PLL, decoupling, design, layout and optimization methodology. However, there is absolutely no indication how any of this relates to the claimed single cell including a signal processing circuit, a buffer circuit for buffering a signal external to the integrated circuit bearing the cell, and layout information. Where, in Luk, or any of the other applied references, is the examiner alleging a teaching of a buffer circuit for buffering a signal external to the integrated circuit bearing the single cell? The examiner does not expressly say.

Even in the examiner's response, at pages 11 et seq. of the answer, the examiner merely lists elements of claim 1 and alleges that Luk teaches these limitations in Figure 9 and concluding that "both Luk . . . and the instant claimed invention are the same" (answer, page 14). But, again, no explicit indication is

made by the examiner as to where, in Luk, or any other applied reference, is shown the buffer circuit, as claimed.

While the instant claims may appear to be broad, the initial burden is on the examiner to show unpatentability. By failing to show where any of the applied references discloses or suggests a single cell including a signal processing circuit, a buffer circuit for buffering a signal external to the integrated circuit in which the cell is included, and layout information, as claimed, the examiner has failed to establish a prima facie case of anticipation.

Accordingly, we will not sustain the rejection of claims 1-30 under either 35 U.S.C. §102(e) or (b). The examiner's decision is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MAHSHID D. SAADAT Administrative Patent Judge	)	

EAK:clm

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